



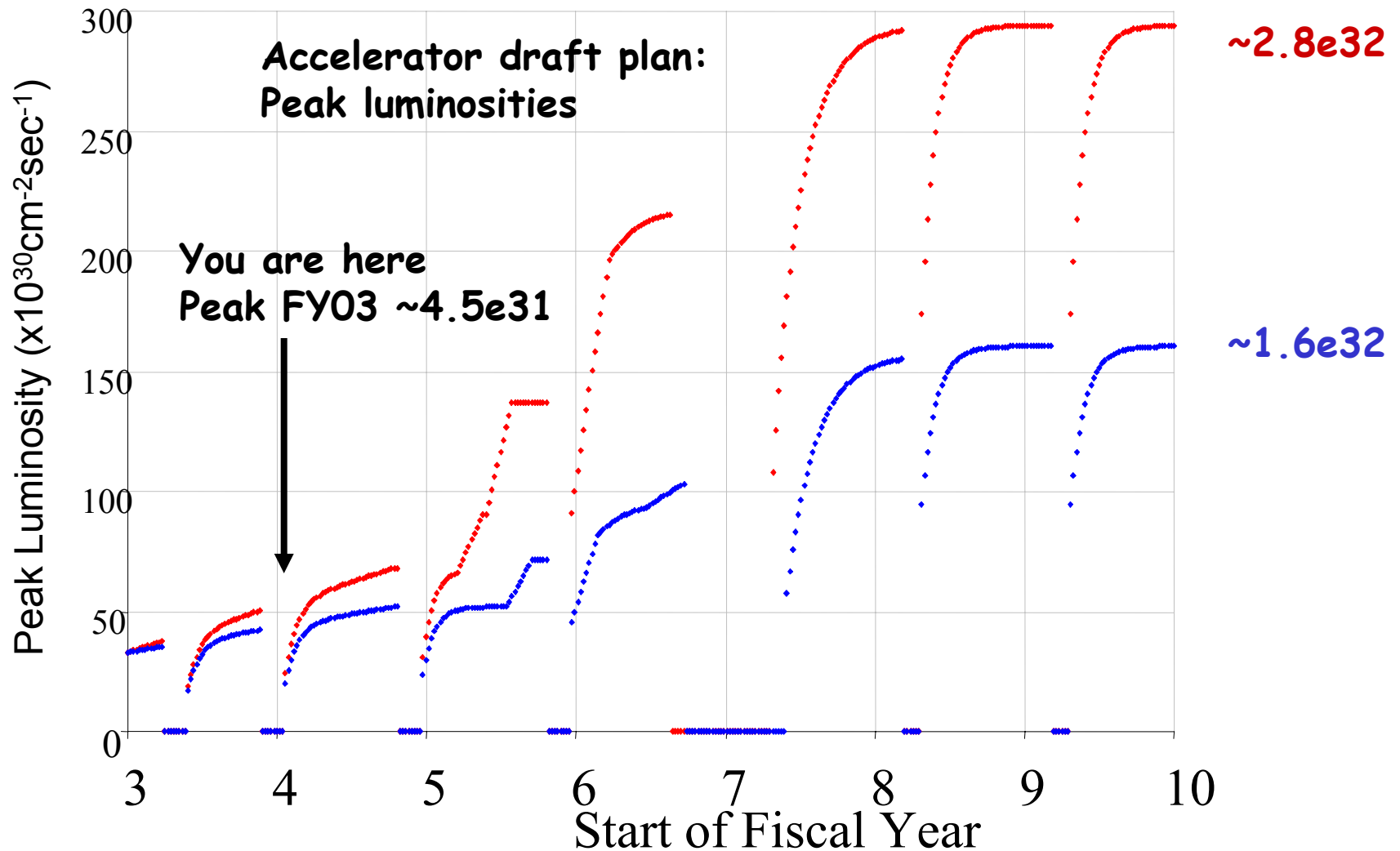
DØ RunIIb Trigger and DAQ/Online Upgrades

WBS 1.2, WBS 1.3

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for the DØ Trigger Upgrade Group



Run IIb Luminosity Projections





Ingredients of the Trigger Upgrade

- Level 1
 - ◆ Calorimeter trigger upgrade
 - ▲ sharpens turn-on trigger thresholds
 - ▲ more topological cuts
 - ◆ Calorimeter track-match
 - ▲ fake EM rejection
 - ▲ tau trigger
 - ◆ L1 tracking trigger upgrade (CTT)
 - ▲ improved tracking rejection especially at higher occupancies
 - ▲ inputs to Calorimeter track-match
- Level 2
 - ◆ L2 Processor upgrades for more complex algorithms
 - ◆ Silicon Track Trigger expansion
 - ▲ More processing power
 - ▲ use trigger inputs from new silicon layer 0
- Upgrade/maintain DAQ/Online systems



Benchmark Trigger Menu

- Core trigger menu, simulated at $L=2e32$, $\Delta t=396$ ns

Trigger	Example Physics Channels	L1 Rate (kHz) (no upgrade)	L1 Rate (kHz) (with upgrade)
EM (1 EM TT > 10 GeV)	$W \rightarrow e\nu$, SUSY, $WH \rightarrow evjj$	1.3	0.7
Di-EM (1 EM TT > 7 GeV, 2 EM TT > 5 GeV)	$Z \rightarrow ee$, $W\gamma$, SUSY $ZH \rightarrow eejj$	0.5	0.1
Muon (muon $p_T > 11$ GeV + CFT Track)	$W \rightarrow \mu\nu$ $WH \rightarrow \mu\nu jj$	6	0.4
Di-Muons (2 muons $p_T > 3$ GeV + CFT Tracks)	$Z \rightarrow \mu\mu$, $J/\Psi \rightarrow \mu\mu$ $ZH \rightarrow \mu\mu jj$	0.4	< 0.1
Electron + Jets (1 EM TT > 7 GeV, 2 Had TT > 5 GeV)	$WH \rightarrow e\nu+jets$ $tt \rightarrow e\nu+jets$	0.8	0.2
Muon + Jet (muon $p_T > 3$ GeV, 1 Had TT > 5 GeV)	$WH \rightarrow \mu\nu+jets$ $tt \rightarrow \mu\nu+jets$	< 0.1	< 0.1
Jet+MET (2 TT > 5 GeV, Missing $E_T > 10$ GeV)	$ZH \rightarrow \nu\bar{\nu}b\bar{b}$, SUSY	2.1	0.8
Muon + EM (muons $p_T > 3$ GeV+ CFT track + 1 EM TT > 5 GeV)	$H \rightarrow WW, ZZ$	< 0.1	< 0.1
Single Isolated Track (1 Isolated CFT track, $p_T > 10$ GeV)	$H \rightarrow \tau\tau$, $W \rightarrow \mu\nu$	17	1.0
Di-Track (1 isolated tracks $p_T > 10$ GeV, 2 tracks $p_T > 5$ GeV, 1 matched with EM energy)	$H \rightarrow \tau\tau$, SUSY	0.6	< 0.1

Total L1 bandwidth
= ~5 kHz

Additional
headroom
available from

- topological
cuts available in
upgraded L1cal

- Higher mu p_T
threshold with
upgraded CTT

Total rate:

~30 kHz

3.2 kHz



Trigger Upgrade Project Institutions

Sub-project	Institution(s)
Calorimeter: ADF	(Saclay), MSU, UIC*, Virginia*
Calorimeter: TAB	Columbia
Track trigger	Boston U., FNAL
Cal-Track match	U. of Arizona
Simulation & algorithms	Notre Dame, Saclay, Kansas, Manchester, Brown
Online software & integration	MSU, Northeastern, FSU, Langston
Level 2 β	Orsay, Virginia, MSU
STT upgrade	Boston, Columbia, Stony Brook, FSU

*Recently added



Management structure: Trigger

WBS 1.2: Trigger Upgrade
P. Padley (Rice), D. Wood (Northeastern)

WBS 1.2.1: Level 1 Calorimeter
M. Abolins (MSU), H. Evans (Columbia)

WBS 1.2.2: Level 1 Cal-track match
K. Johns (Arizona)

WBS 1.2.3: Level 1 Tracking
M. Narain (Boston)

WBS 1.2.4: Level 2 Beta upgrade
R. Hirosky (Virginia)

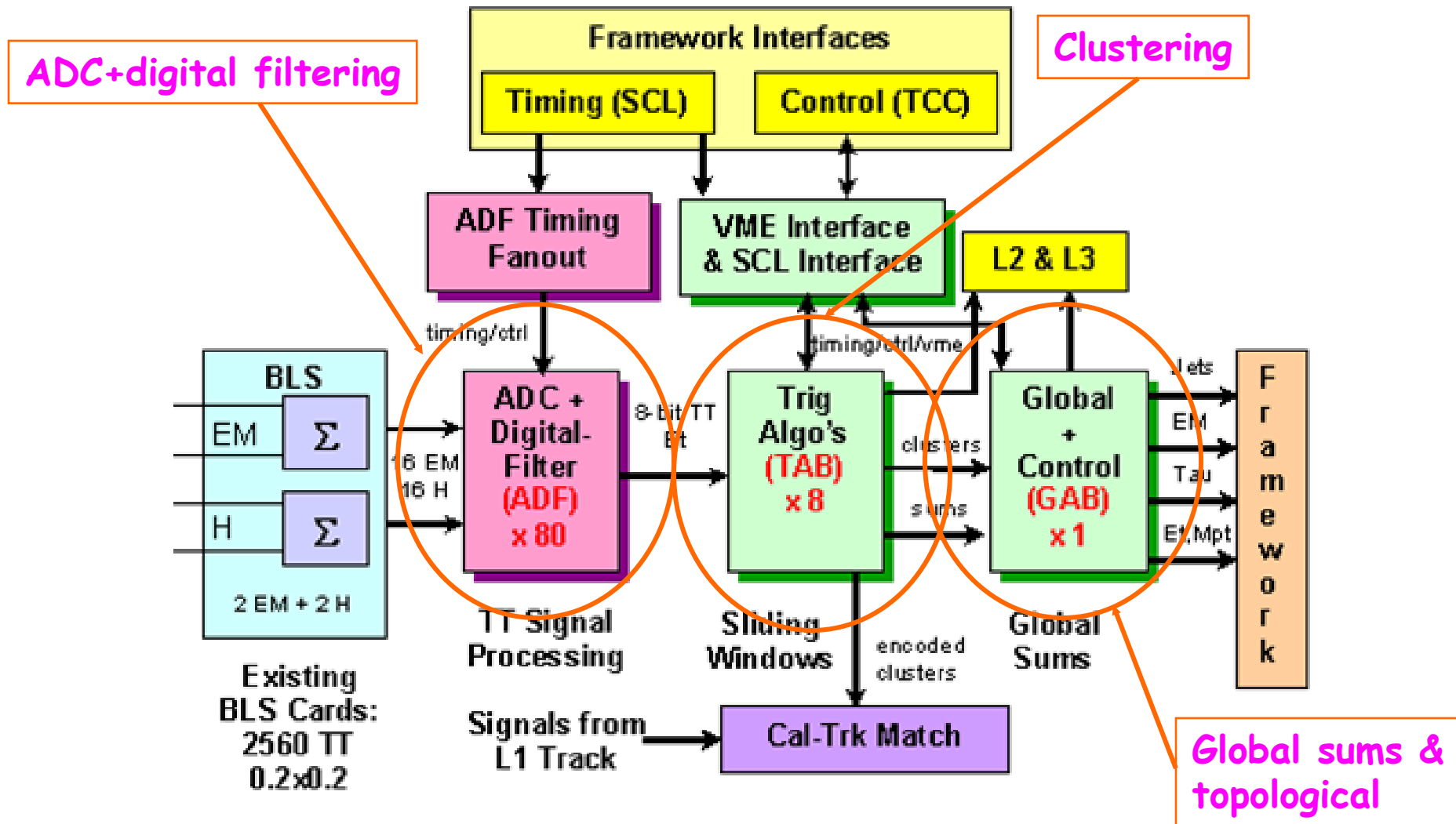
WBS 1.2.5: Level 2 STT upgrade
U. Heintz (Boston)

WBS 1.2.6: Trigger Simulation
M. Hildreth (ND), E. Perez (Saclay)

WBS 1.2.8: AFE upgrade
A. Bross (FNAL), TBD

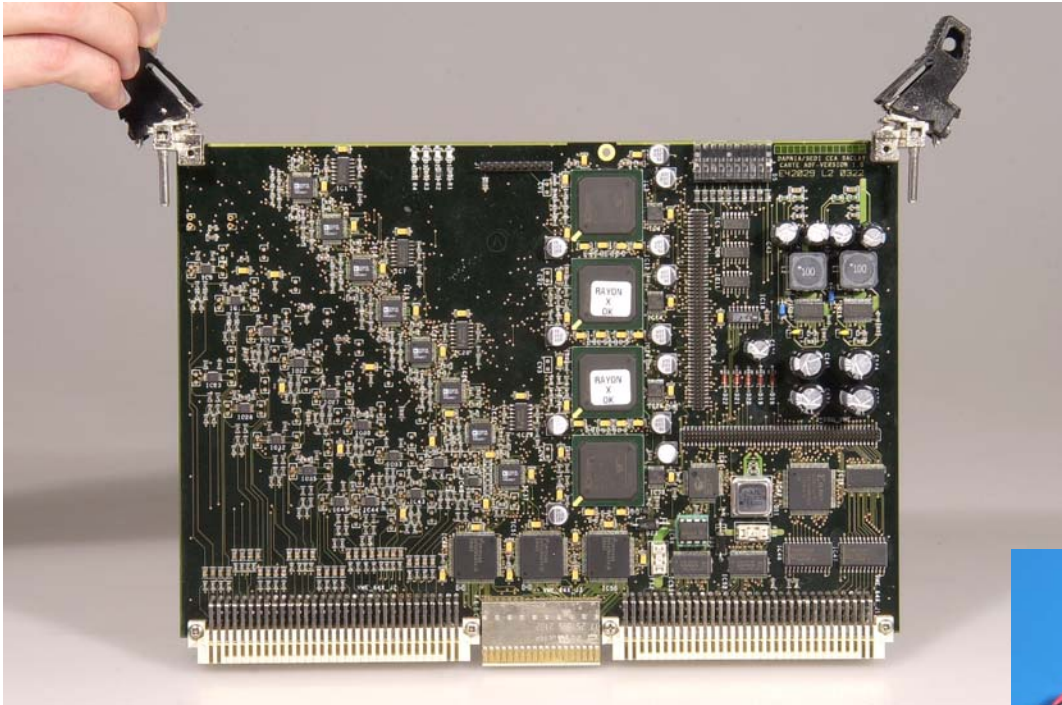


WBS 1.2.1: L1Cal





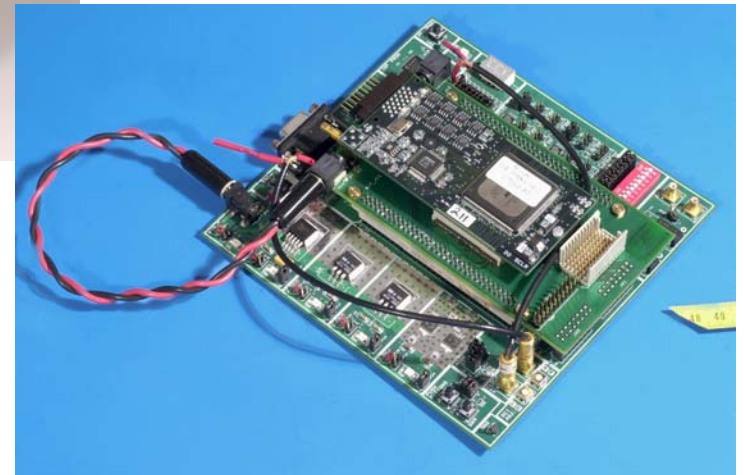
ADF Prototype



ADF Prototype board

Underwent integration tests at Fermilab, Oct 03

Prototype ADF Timing Card



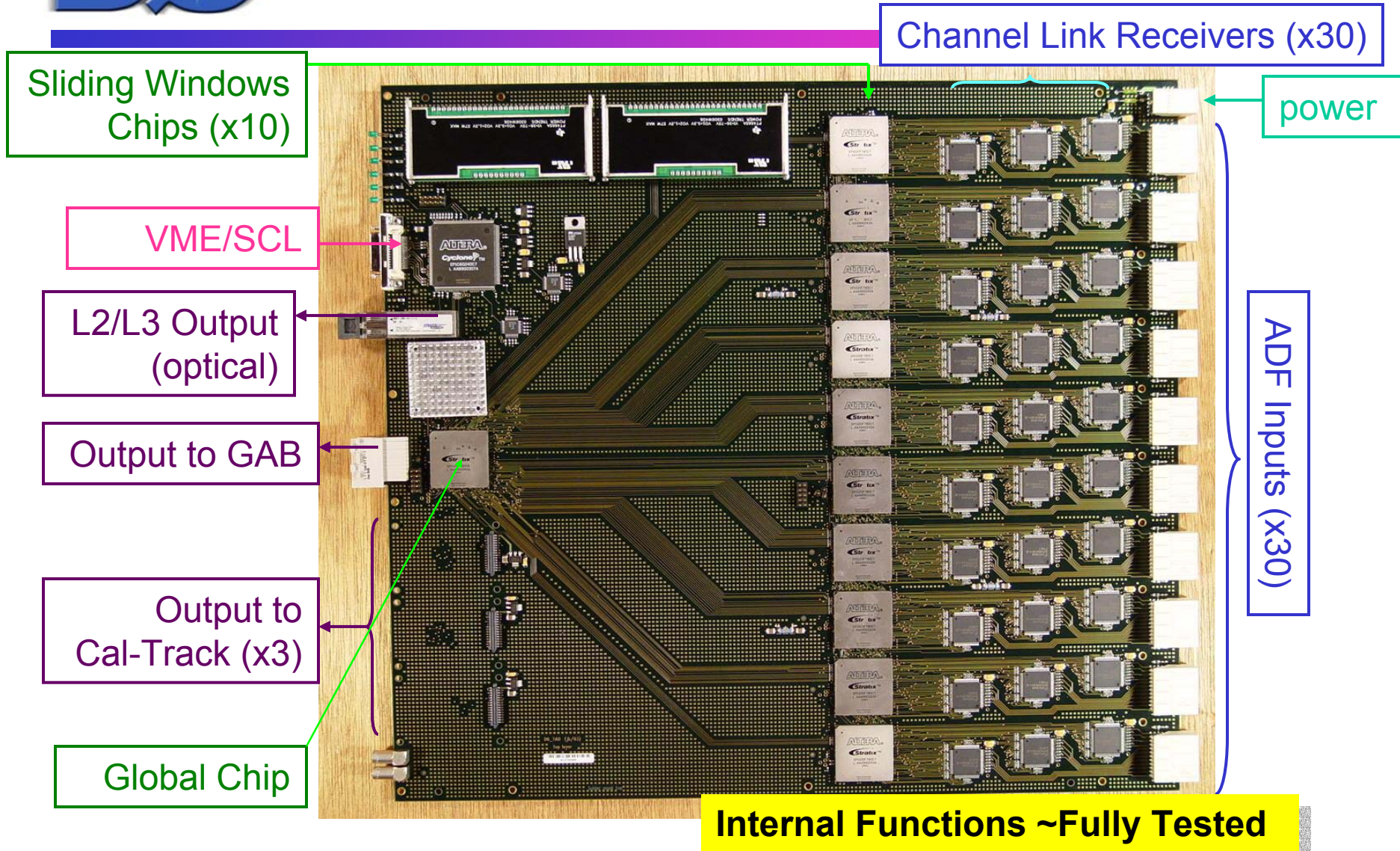


ADF future plans

- Note that the Saclay group will not be able to participate in DØ beyond the prototyping phase
 - ♦ Thanks to Saclay to bringing the ADF this far
 - ♦ Thanks to MSU for agreeing to take over the ADF
 - ♦ UIC and Virginia added to the ADF effort
- Next layout of the ADF will be done jointly by Saclay and MSU engineers. Once working, MSU takes ownership



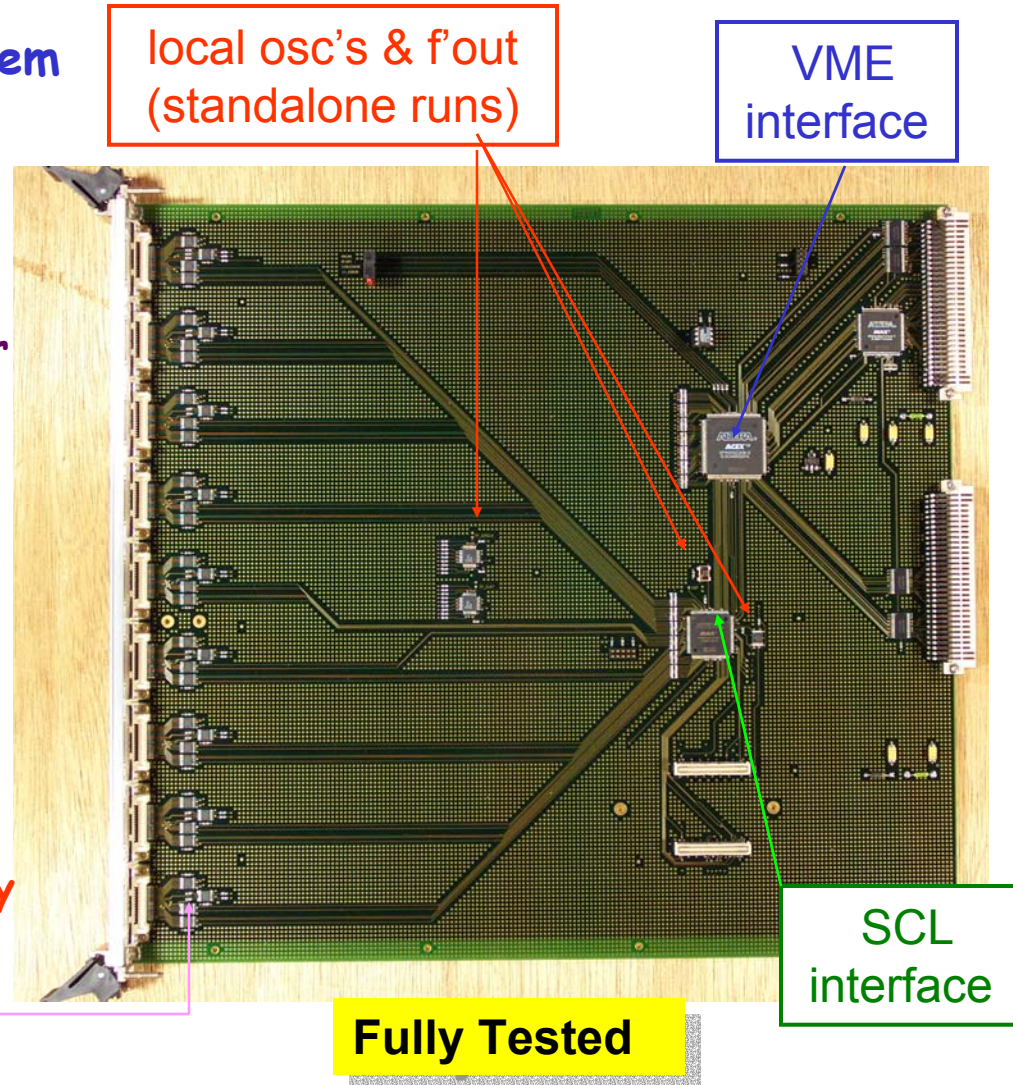
TAB Prototype





VME/SCL Board

- New Comp. of TAB/GAB system
 - ♦ proposed: Feb 03
 - ♦ change control: Mar 03
- Interfaces to
 - ♦ VME (custom protocol)
 - ▲ not enough space on TAB for standard VME
 - ♦ DØ Trigger Timing (SCL)
 - ♦ (previously part of GAB)
- Why Split off from GAB
 - ♦ simplifies system design & maintenance
 - ♦ allows speedy testing of prototype TAB
- Prototype at Nevis: May 12
 - ♦ main VME & SCL functionality tested & working





TAB/GAB Test Card

TAB/GAB Data Rates

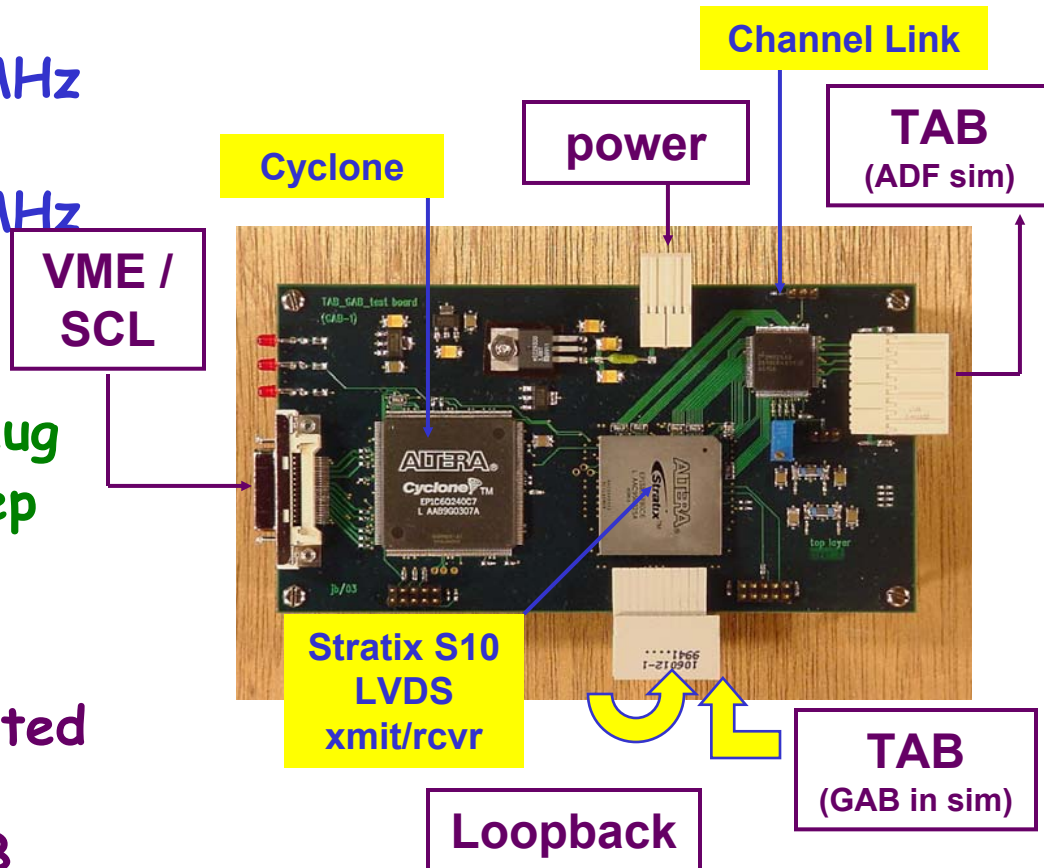
- ◆ TAB: LVDS 424 MHz
 - ▲ (channel link)
- ◆ GAB: LVDS 636 MHz
 - ▲ (stratix)

Test Card at Nevis

- ◆ Start Design mid-Aug
- ◆ Board at Nevis 29-Sep
- ◆ Cost ~\$2K

• Status

- ◆ ADF-to-TAB xmit tested before integration
- ◆ Will test TAB-to-GAB before sending out GAB for fabrication





Prototype Integration Tests

- First test of Serial Command Link (SCL) → TAB done in 9-17 October
- Tests with ADF + TAB prototypes
 - ♦ SCL → VME/SCL → TAB, ADF
 - ♦ BLS Data (split) → ADF → TAB
 - ♦ Flexible, staged schedule allows components to be included as they become available
- Set up semi-permanent Test Area outside of Movable Counting House
 - ♦ connection to SCL, split data signals
 - ♦ allows L1Cal tests without disturbing Run IIa data taking

Successful integration tests last month

ADF-→TAB

TAB -> L1mu (L1cal-track surrogate)



WBS 1.2.2: L1 cal-track matching

- **MTCxx (Trigger Cards)**
 - ♦ Preproduction design complete
 - ♦ Layout and final checks in progress
 - ♦ Goal is to submit in November 03
- **UFB (Flavor Board)**
 - ♦ Prototypes in hand
 - ♦ See next Slide
- **MTCM (Crate Manger)**
 - ♦ Logic changes finished
 - ♦ Awaiting final checks



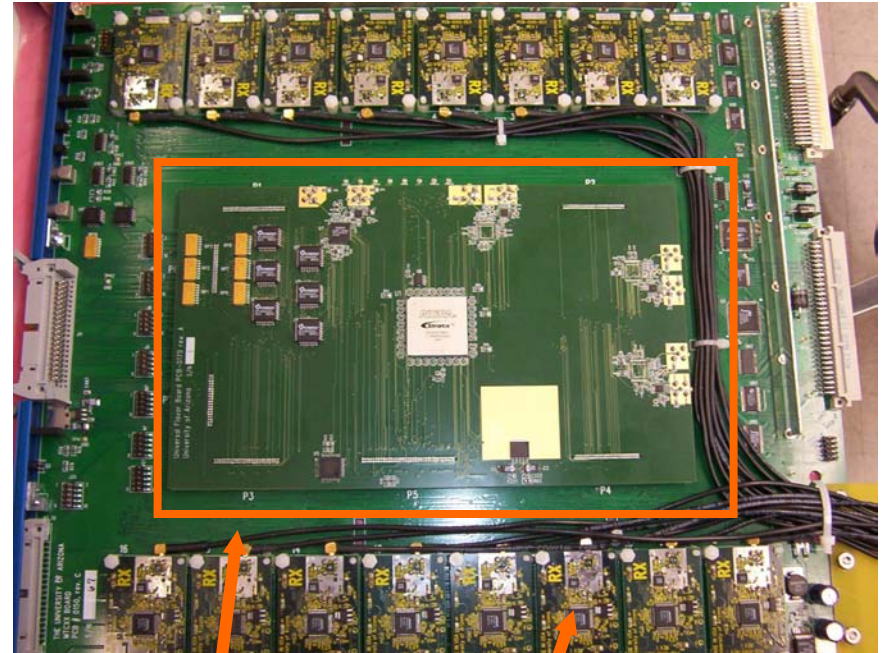
L1 Cal Track Match

- UFB (Flavor Board)

- ◆ Prototypes in hand
- ◆ Boundary scan and downloading OK
- ◆ Receiver/transmitter testing in progress
- ◆ L1MU "05" algorithm implemented in Stratix EP1S20F780C7

- ▲ (simulated but not tested)

- ◆ $H \rightarrow \tau\tau$ algorithm implementation in progress



MTCxx (mother)
Run IIa version

Universal Flavor board (daughter)
Run IIb prototype



L1CalTrack Status

- Infrastructure

- ♦ VME crates, processors, power supplies, cables in hand
- ♦ L1CTT to L1CalTrack cables installed during current shutdown (not terminated)
- ♦ Crates installed in Movable Counting House

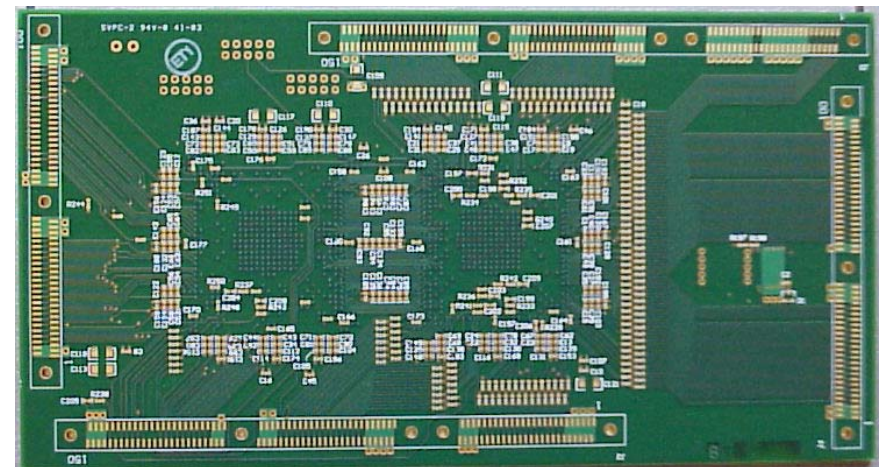
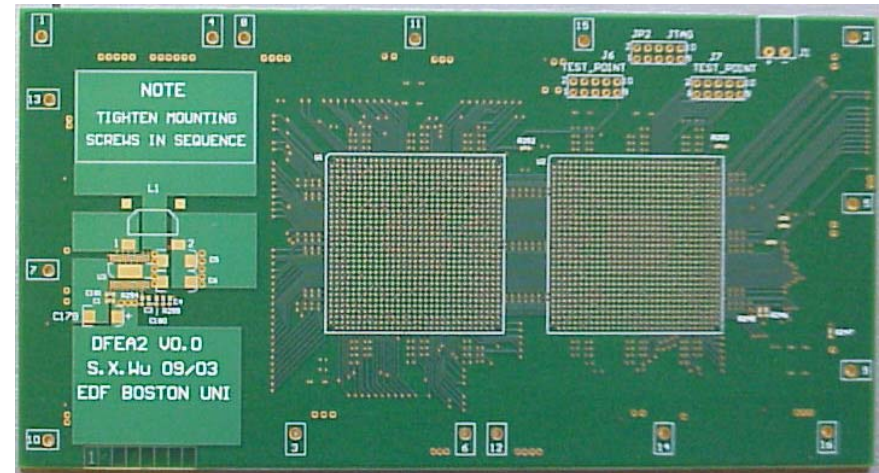
- Commissioning

- ♦ Plan is to use spare L1MU cards in L1CalTrack crates to establish communication with Trigger Framework and L3
- ♦ Replace spares with L1CalTrack cards as available



L1 CTT

- **Prototype DFEA:**
 - ◆ 10/17/03 prototype PCB returned
 - ◆ Currently being stuffed





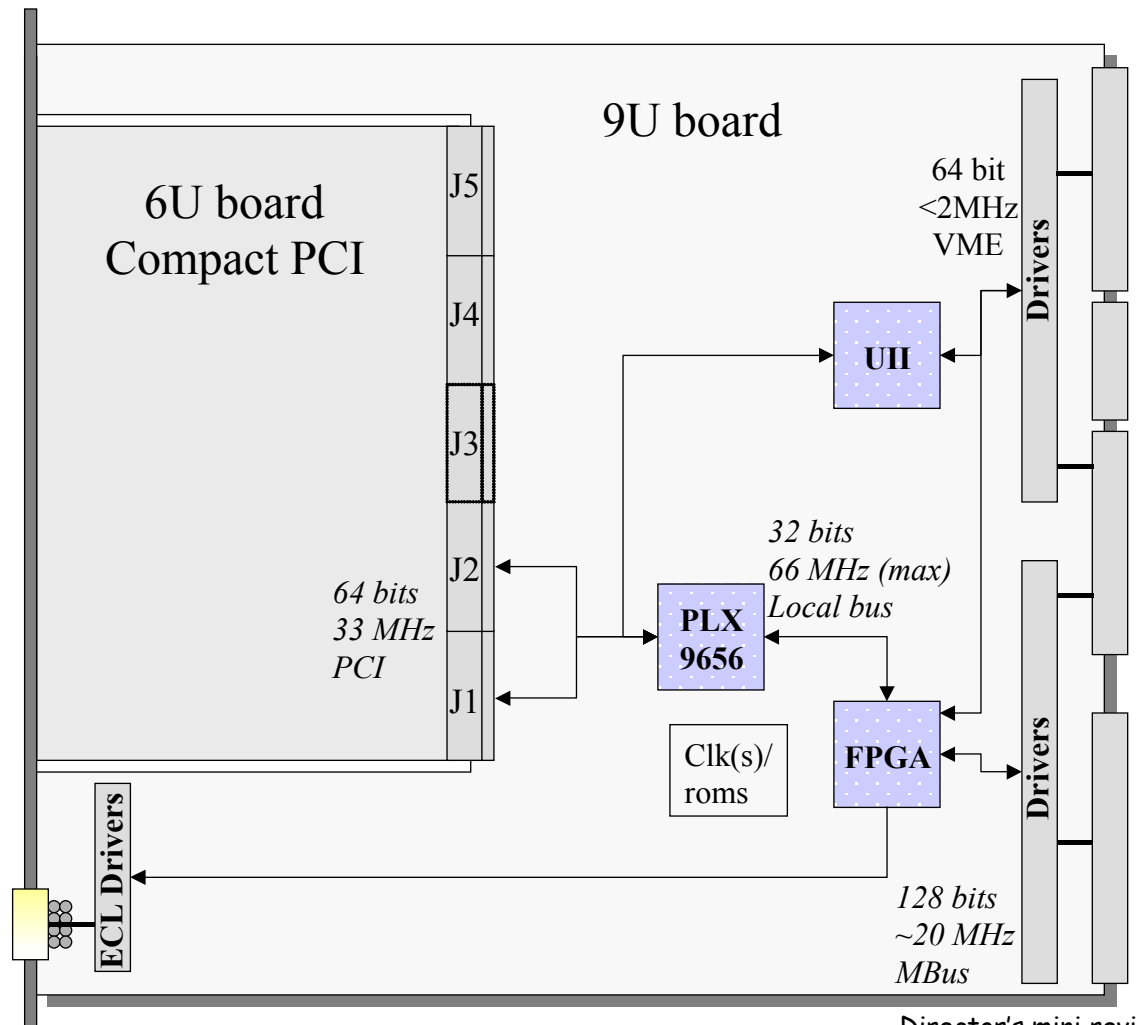
WBS 1.2.3: L1 CTT

- Digital Front End Axial (DFEA) daughter cards get replaced with new layout with larger FPGA's (Xilinx Virtex-II XC2V6000)
 - ♦ Only 80 daughter cards get replaced;
 - ♦ rest of Run IIa system remains intact
- Implemented prototype firmware (Boston U)
 - ♦ Includes equation files from all 4 momentum bins
 - ▲ $p_T > 10 \text{ GeV}$, $5 < p_T < 10 \text{ GeV}$, $3 < p_T < 5 \text{ GeV}$,
 $1.5 < p_T < 3 \text{ GeV}$
 - ♦ DFEA logic is implemented in two FPGAs



WBS 1.2.4: L2 β eta Upgrade

- Run IIa Betas are installed and running
- Run IIb strategy: purchase additional, more powerful commercial processors as late as reasonably possible.



Director's mini review
of DØ upgrades
Nov 5th, 2003

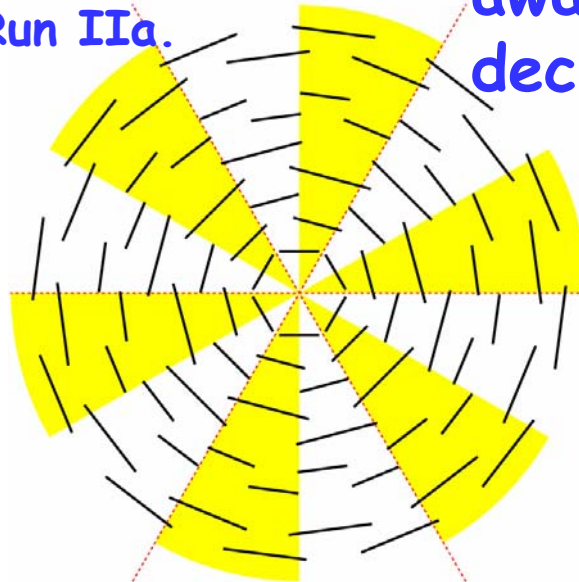


WBS 1.2.5: Silicon Track Trigger for Run IIb

- STT upgrade needed to
 - ◆ accommodate new L0
 - ◆ New L0 fits within baseline Run IIb upgrade
 - ◆ even without L0, increase processing power for higher occupancy
- Modest STT upgrade requires small quantity of same boards that are used in Run IIa.

Technical Progress:

- VME Transition Modules procured
 - ◆ Concern about obsolescence
- Other procurements awaiting Layer 0 decision





Trigger Installation: Minimal Downtime

- Only upgrade that needs detector access is the CTT
 - ◆ This can be done with a series of short accesses during normal accelerator downtimes.
 - ▲ Install a card during a downtime
 - ▲ Load Run 2a algorithms
 - ▲ Commission the board, if it fails, only 1/48th of the track trigger affected.
 - ◆ Essentially no impact on running
- L1Cal upgrade requires detector downtime
 - ◆ No cal trigger to DØ for 10 weeks.
 - ◆ Installation should coincide with a normal accelerator shutdown period



WBS 1.3: DAQ/Online

System	Items	Need
Level 3 filter nodes	96 more L3 Farm nodes	Match to rates and processing requirements
DAQ HOST system	Linux data logging nodes and buffer disk arrays	Replace existing systems with higher performance nodes
ORACLE systems	Database nodes, disk arrays, and backup systems	Adopt lab standard ORACLE platform
File Server systems	Linux server nodes, disk arrays, and backup systems	Provide increased storage capacity
Slow Control system	VME processors for control and monitoring of detector	Improve monitoring performance for extended run

Upgrades to DAQ/Online systems required for long-term, high rate running during Run IIb



Management structure: DAQ/Online

WBS 1.3: DAQ/Online

S.Fuess (FNAL), P. Slattery (Rochester)

WBS 1.3.1: Level 3 Systems

D. Chapin (Brown), G. Watts (UWashington)

WBS 1.3.2: Network & Host Systems

J. Fitzmaurice (FNAL), S. Drzywdzinski (FNAL)

WBS 1.3.3: Control Systems

F. Bartlett (FNAL), G. Savage (FNAL),
V. Sirotenko (FNAL)

WBS 1.3.4: DAQ/Online Management

(P. Slattery)



WBS 1.3: DAQ/Online

System	Status
Level 3 filter nodes	Current number of L3 farm nodes is expected to be sufficient for FY04. Watching CD farm purchase procedure as model to follow for scheduled FY05 purchase.
DAQ HOST system	1 st DAQ Host system, quad Linux node, being commissioned. 2 more (of 6 total) servers to be purchased in Fall/Winter 2003.
ORACLE systems	Have run a Linux ORACLE 8i installation for ~ 6 months. Will install 9i system in Fall/Winter 2003.
File Server systems	Testing Fibre Channel SAN and RAID array I/O rates. Testing prototypes in preparation for Spring 2004 purchases.
Slow Control system	Performing EPICS software updates to keep current with community developments. Planning tests on Intel processors in Spring 2004.



Summary

- Trigger and DAQ upgrades proceeding at full speed
- Prototypes in hand:
 - ♦ L1cal: splitter, TAB, VME/SCL, ADF
 - ♦ Cal-track: UFB
 - ♦ L1CTT: DFEA preproduction I (in assembly house)
- Major milestones achieved in integration tests in July-Oct
 - ♦ Run off of DØ timing signals
 - ♦ Data sent between ADF and TAB
 - ♦ Data sent between TAB and cal-track surrogate (L1mu) - generated triggers in DØ just as it was supposed to
- Plan to install with minimal downtime